# PowerBrick™6.0

User's Manual
Edition 4.0

***4 Generation Intel® i7 Industrial Computer***

**Acura Embedded Systems Inc.**

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# 1.0 INTRODUCTION

## Specification

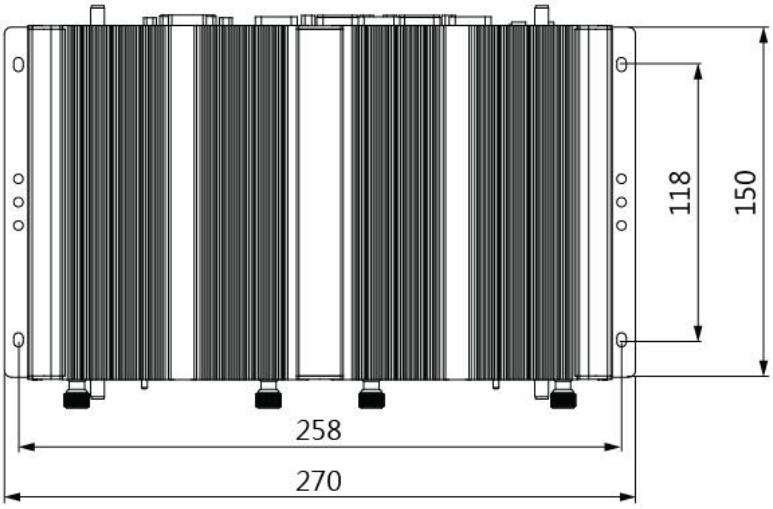
| | |
|---|---|
| **System** | |
| CPU | Intel Gen 4 Core i7-4650U 1.7GHz up to 3.3GHz |
| Memory | 2 x DDR3L 1600 MHz SO-DIMM up to 16GB |
| Chipset | QM87 |
| LAN Chipset | Intel I210-AT Gb/s Ethernet Controllers Onboard<br>Support POE |
| Audio | Realtek ALC662 HD Codec onboard |
| Watchdog | Watchdog Timer Support, Offer 1 – 255 Step |
| **Power Requirement** | |
| Power Input | 9V-36V DC Power input |
| Power Protection | Automatics Recovery Short Circuit Protection |
| Power Management | Vehicle Power Ignition for Variety Vehicle |
| Power Off Control | Power off Delay Time Setting by Software, Default is 2 Seconds. |
| Battery | Internal Battery Kit for 10 Mins Operating (Optional) |
| **Storage** | |
| Type | 2 x 2.5” Drive Bay for SATA Type HDD / SSD, Support RAID 0, 1<br>1 x Mini-PCIe DOM |

| | |
|---|---|
| **Graphics** | |
| Graphics | Intel® HD Graphics 5000<br>DirectX Video Acceleration (DXVA) for Accelerating Video Processing Full- AVC/VC1/MPEG2 HW Decode<br>Supports DirectX 11/10.1/10/9 and OpenGL 4.0 |
| Resolution | Up to 4096 x 2304 |
| **Qualification** | |
| Certifications | CE, FCC Class A, EMark Compliance, EN50155, EN50121 |
| **I/O** | |
| Serial Port | 4 x RS-232 (2 with RS-485 (Auto Direction Control)) |
| USB Port | 2 x USB 3.0 Ports, 2 x USB 2.0 Ports |
| LAN | 4 x Ports for GbE POE (15.4W per port) |
| Video Port | 1 x VGA Connector on Rear I/O ;1 x DVI-I Connector on Rear I/O<br>1 x DP Port Connector on Rear I/O<br>(Support Dual Independent Display) |
| DIO Port | 4 In and 4 Out |
| Audio | 1 x Line-out and 1 x Mic-in (Line-in Optional) |
| SIM Card Socket | 1 x SIM Card Socket Supported Onboard with eject |
| **Environment** | |
| Operating Temp. | -40ºC ~ 70ºC (Default CPU 17Watt) |
| Storage Temp. | -40ºC~ 80ºC |
| Relative Humidity | 0% RH– 95% RH |
| Vibration (random) | 2.5g@5~500 Hz with SSD |
| Vibration Operating | MIL-STD-810F, Method 514.5, Category 20, Ground Vehicle-Highway |
| Truck Storage | MIL-STD-810F, Method 514.5, Category 24, Integrity Test |
| Shock | Operating: MIL-STD-810F, Method 516.5, Procedure I,<br>Trucks and semi-trailers=40G (11ms) with SSD |
| Crash Hazard | MIL-STD-810F, Method 516.5, Procedure V,<br>Ground equipment=100 |
| **Mechanical** | |
| Construction | Aluminum alloy |
| Mounting | Supports both of wall-mount/VESA-mount |
| Weight | 1.780 kg ( 3.92 LBs) |
| Dimensions | 250 x 150 x 55 mm |

## System


GPS
LAN 2
LAN 4
LAN 1
LAN 3
ACURA
COM 3
DIO
SIM CARD
POWER
UPS HDD
WWAN ACC
3G / LTE


COM 2
COM 4 / DVR
VGA
LAN 2
LAN 1
COM 1
DP
DVI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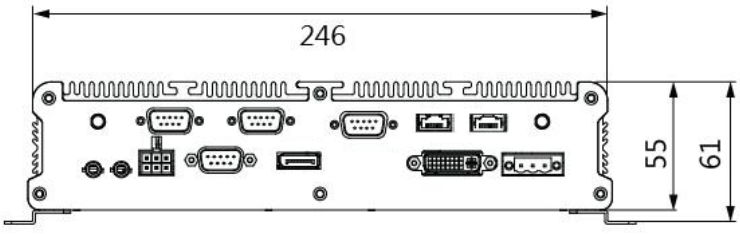
258
270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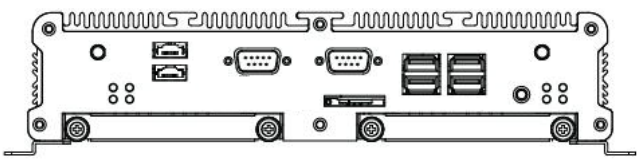
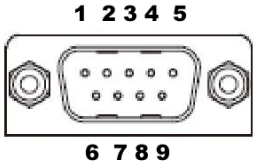


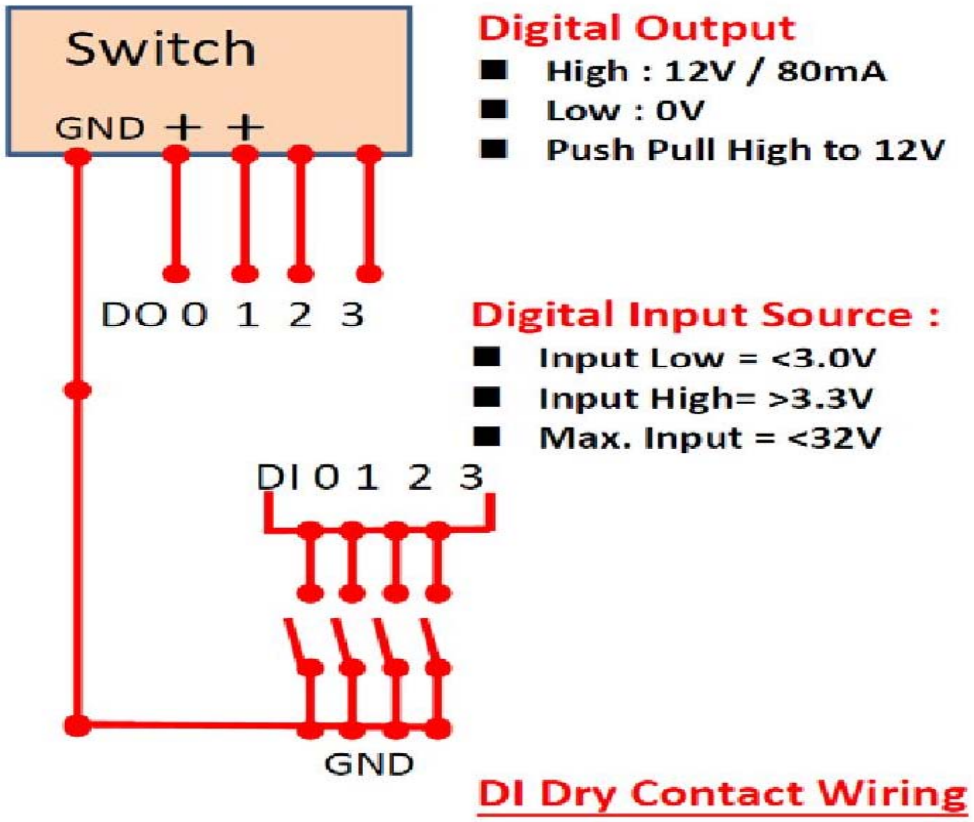
## 2.0 IMPORTANT CONNECTOR

### 2.1 GPIO Connector



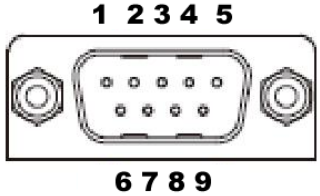

GPIO Pin Definition

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GPI0 | 2 | GPI1 |
| 3 | GPI2 | 4 | GPI3 |
| 5 | GPO0 | 6 | GPO1 |
| 7 | GPO2 | 8 | GPO3 |
| 9 | GND | | |




### 2.2 COM Port Connector (COM)

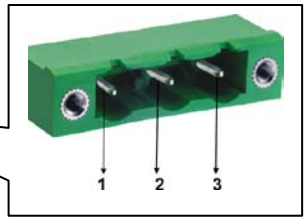
Connector pin
**COM 1,2,3,4**




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | COM1,2,3,4_DCD (COM1,2_RS-485_TXD-/RXD-) | 2 | COM1,2,3,4_RXD (Com1,2_RS-485_TXD+/RXD+) |
| 3 | COM_TXD | 4 | COM_DTR |
| 5 | GND | 6 | COM_DSR |
| 7 | COM_RTS | 8 | COM_CTS |
| 9 | COM_RI# | | |

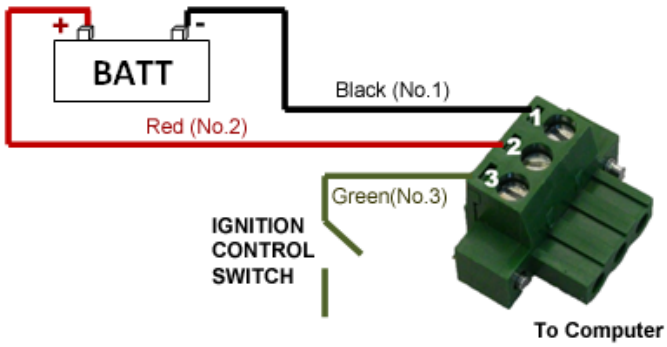
## 2.3 Power Input Connector

**Power Input**




| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | VIN (9-36V) |
| 3 | IGNITION |

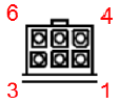
Power Brick 6.0 Power Wiring



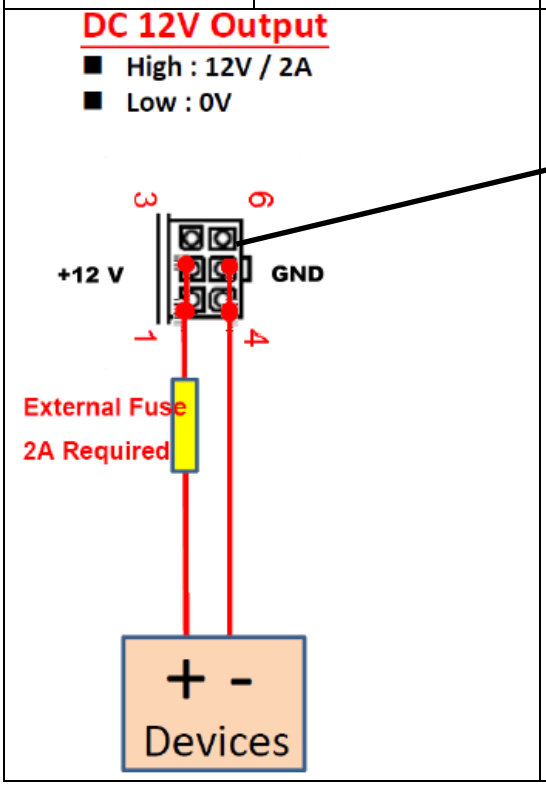

## 2.4 ATX 6PIN Connector (POWER OUT)

Connector location

**Power Out**




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +12V | 2 | +12V |
| 3 | EXT_DI1 | 4 | GND |
| 5 | GND | 6 | EXT_DI2 |

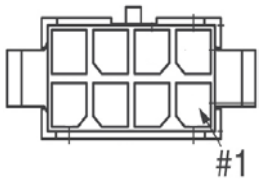



## 2.5 WM1780-ND Connecting to the Network

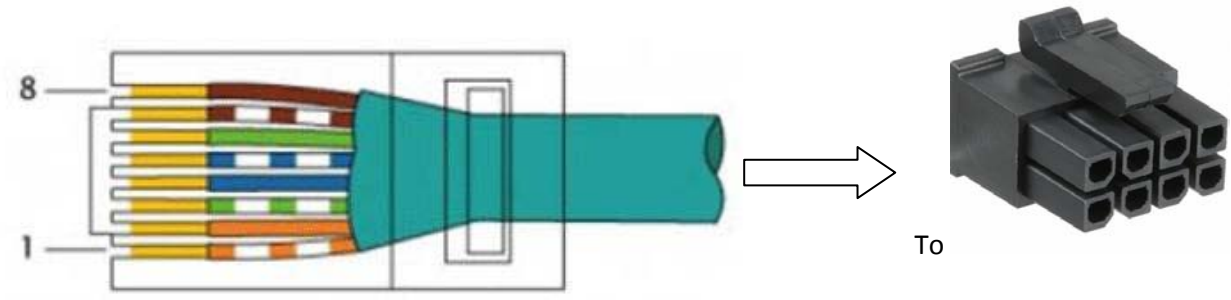
A. WM1780-ND to RJ45 Cable


B. WM1780-ND connector pin define

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TD1+ | 2 | TD1- |
| 3 | TD2+ | 4 | TD3+ |
| 5 | TD3- | 6 | TD2- |
| 7 | TD4+ | 8 | TD4- |




C. CAT5 connector pin define




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TD1+ | 2 | TD1- |
| 3 | TD2+ | 4 | TD3+ |
| 5 | TD3- | 6 | TD2- |
| 7 | TD4+ | 8 | TD4- |

## 3.0 Ignition Power Management (Optional)

**Startup/shutdown conditions from the IGNITION signal:**

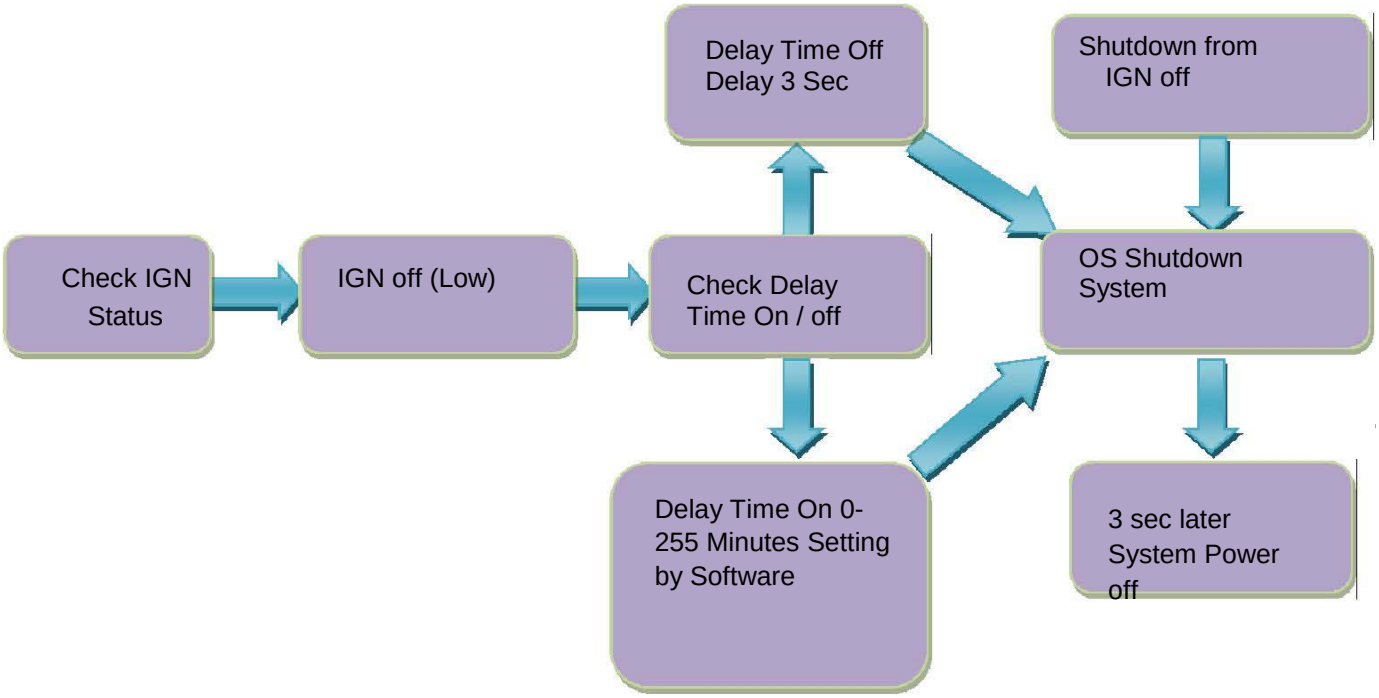
- IGNITION startup signal must be valid during 3 sec. (anti-noise protection).
- IGNITION shutdown – IGNITION signal must be inactive during 3 Sec, then PIC controller initiate Power Button signal (**OS must be set to shut down from the Power Button**). It generate Main Button shutdown event and then goes to complete power off.

Typically the system can start only from IGNITION signal, because startup PIC controller is disconnected from the power source.

The system can be switched off from:

- Power IGNITION OFF signal.
- ACPI OS shutdown
- Power Button – generate ACPI event (OS dependent).


**Power Ignition Startup Procedure**




**Power Ignition Shutdown Procedure**

**Power Management**

- Power-off delay time is selectable by Software to disable and enable in 0-255 minutes
- Ignition On/Off status detectable by IGNITION CONTROL SWITCH.
- If the ignition is off and the system is still on after 3 Sec, PowerBrick 6.0 will shut down automatically.
- If the ignition is turned on again and the power-off delay is in progress, PowerBrick 6.0 will cancel the delay function and will continue to operate normally.
- If the ignition is turned on again and the power-off delay ended, PowerBrick 6.0 will shut down completely will power-on again automatically.

## 4.0 GPIO & Delay Time Setting

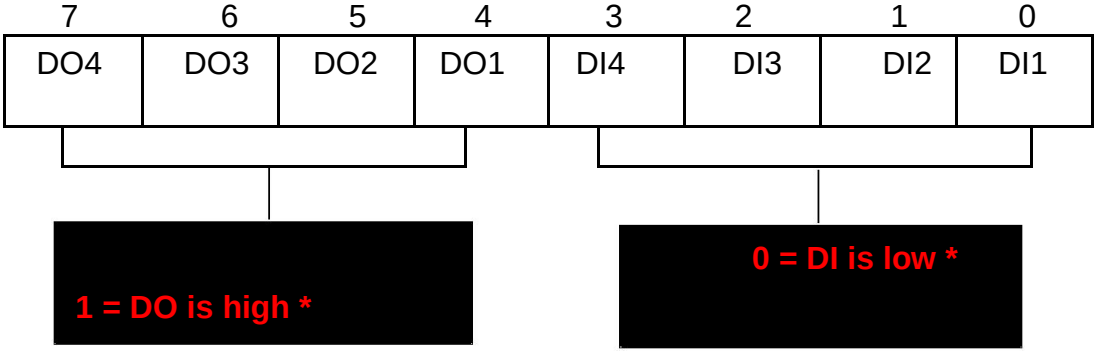
### 4.1 GPIO and Ignition Control Register

The General Purpose I/O is an interface available on some devices. These can read digital signals from other parts of a circuit, or output to control other devices. At GPIO control register, the GPI is use to receive data, the GPO is set data to send.

**I/O port:** **0xA35 (base address)** for Control Register (Read 0xA2h / Write 0xA1h)
**0xA36 (base address)** for Control Data Value

**Debug Command Line**

- **O A35 A1**
- **O A36 0F // Set Bit 4-7to Low**




**GPIO5 Output Enable Register – Index A0h**

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | GPIO57_OE | R/W | 0 | 0: GPIO57 is input; 1: GPIO57 is output |
| 6 | GPIO56_OE | R/W | 0 | 0: GPIO56 is input; 1: GPIO56 is output |
| 5 | GPIO55_OE | R/W | 0 | 0: GPIO55 is input; 1: GPIO55 is output |
| 4 | GPIO54_OE | R/W | 0 | 0: GPIO54 is input; 1: GPIO54 is output |
| 3 | GPIO53_OE | R/W | 0 | 0: GPIO53 is input; 1: GPIO53 is output |
| 2 | GPIO52_OE | R/W | 0 | 0: GPIO52 is input; 1: GPIO52 is output |
| 1 | GPIO51_OE | R/W | 0 | 0: GPIO51 is input; 1: GPIO51 is output |
| 0 | GPIO50_OE | R/W | 0 | 0: GPIO50 is input; 1: GPIO50 is output |

### GPIO5 Output Data Register – Index A1h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | GPIO57_DATA | R/W | 1 | GPIO57 output data in output mode. |
| 6 | GPIO56_DATA | R/W | 1 | GPIO56 output data in output mode. |
| 5 | GPIO55_DATA | R/W | 1 | GPIO55 output data in output mode. |
| 4 | GPIO54_DATA | R/W | 1 | GPIO54 output data in output mode. |
| 3 | GPIO53_DATA | R/W | 1 | GPIO53 output data in output mode. |
| 2 | GPIO52_DATA | R/W | 1 | GPIO52 output data in output mode. |
| 1 | GPIO51_DATA | R/W | 1 | GPIO51 output data in output mode. |
| 0 | GPIO50_DATA | R/W | 1 | GPIO50 output data in output mode. |

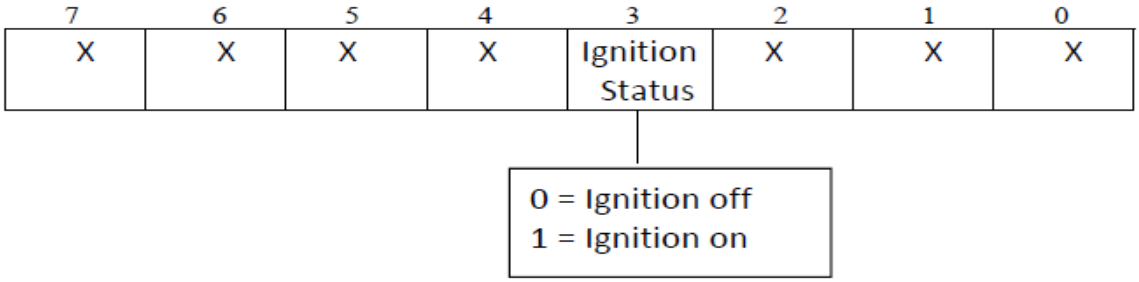
### GPIO5 Pin Status Register – Index A2h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | GPIO57_ST | R | 1 | GPIO57 pin status. |
| 6 | GPIO56_ST | R | 1 | GPIO56 pin status. |
| 5 | GPIO55_ST | R | 1 | GPIO55 pin status. |
| 4 | GPIO54_ST | R | 1 | GPIO54 pin status. |
| 3 | GPIO53_ST | R | 1 | GPIO53 pin status. |
| 2 | GPIO52_ST | R | 1 | GPIO52 pin status. |
| 1 | GPIO51_ST | R | 1 | GPIO51 pin status. |
| 0 | GPIO50_ST | R | 1 | GPIO50 pin status. |

### GPIO5 Drive Enable Register – Index A3h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | GPIO57_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO57 is open drain; 1: GPIO57 is push pull |
| 6 | GPIO56_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO56 is open drain; 1: GPIO56 is push pull |
| 5 | GPIO55_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO55 is open drain; 1: GPIO55 is push pull |
| 4 | GPIO54_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO54 is open drain; 1: GPIO54 is push pull |
| 3 | GPIO53_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO53 is open drain; 1: GPIO53 is push pull |
| 2 | GPIO52_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO52 is open drain; 1: GPIO52 is push pull |
| 1 | GPIO51_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO51 is open drain; 1: GPIO51 is push pull |
| 0 | GPIO50_DRV_ENST | R/W | 0 | GPIO57 Drive Enable<br>0: GPIO50 is open drain; 1: GPIO50 is push pull |

**I/O port: I/O port: 0xA35 (base address)** for Control Register (Read 0xF2h bit 3)
**0xA36 (base address)** for Control Data Value



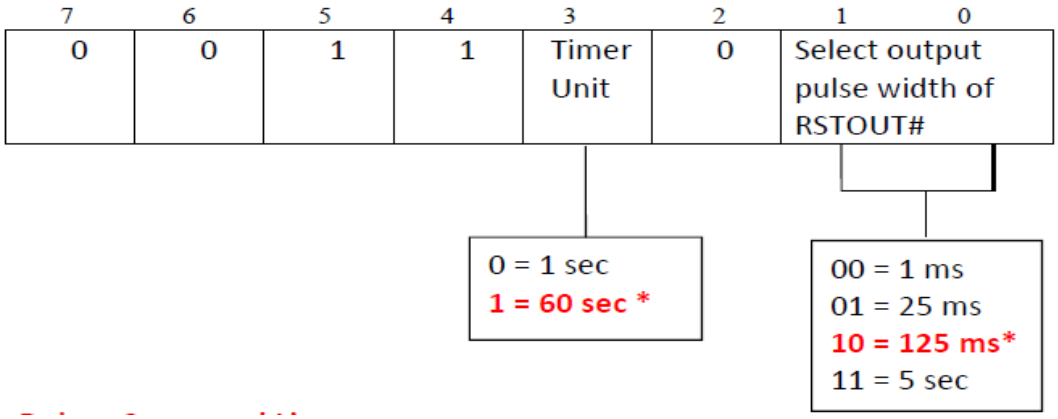

**Debug Command Line**

- O A35 F2
- I A36 // Check Bit 3 Status

## 4.2 WDT Setting

**I/O port: A10 (base address) + 05h and 06h 1 Watchdog Timer Control Register**

The Watchdog Timer Control Register controls the WDT working mode. Write the value to the WDT Configuration Port. The following table describes the Control Register bit definition:




**Debug Command Line**

- **O A16 05**
- **O A15 32 // 5 sec // 3A □5 minutes**

**Watchdog Timer Function**

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

**Watchdog Timer Configuration Register 1-base address +05h**

| Bit | Name | R/W | Default | Description | |
|---|---|---|---|---|---|
| 7 | Reserved | R | 0 | Reserved | |
| 6 | WDTMOUT_STS | R/W | 0 | If watchdog timeout event occurs, this bit will be set to | |
| | | | | 1. Write a 1 to this bit will clear it to 0. | |
| 5 | WD_EN | R/W | 0 | If this bit is set to 1, the counting of watchdog time is | |
| | | | | enabled. | |
| 4 | WD_PULSE | R/W | 0 | Select output mode (0:level, 1:pulse) of RSTOUT# by | |
| | | | | setting this bit. | |
| 3 | WD_UNIT | R/W | 0 | Select time unit (0:1sec, 1:60sec) of watchdog timer by | |
| | | | | setting this bit. | |
| 2 | WD_HACTIVE | R/W | 0 | Select output polarity of RETOUT# (1:high active, 0:low | |
| | | | | active) by setting the bit. | |
| 1-0 | WD_PSWIDTH | R/W | 0 | Select output pulse width of RSTOUT# | |
| | | | | 0:1 ms | 1:25 ms |
| | | | | 2:125 ms | 3:5 sec |

**Watchdog Timer Configuration Register 2-base address +06h**

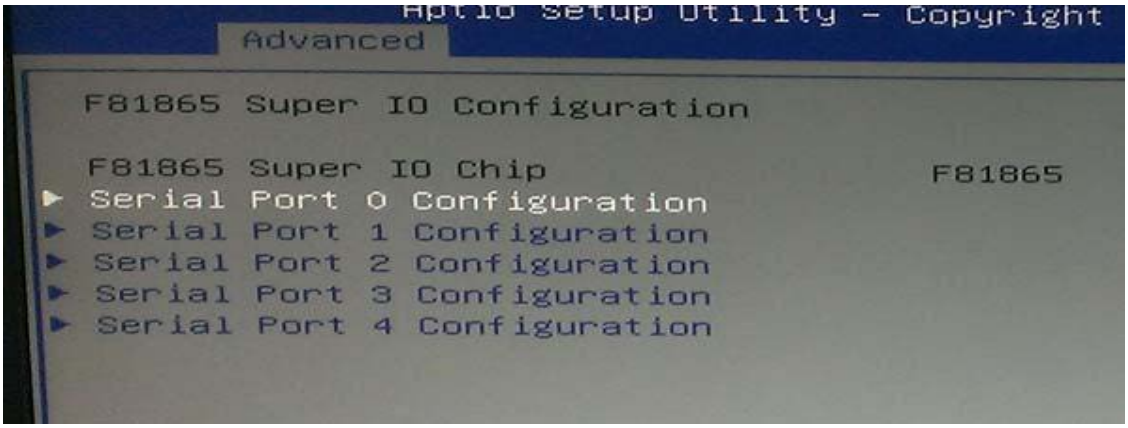
| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | WD_TIME | R/W | 0 | Time of watchdog timer |

**Watchdog PME Control Register -base address + 0Ah**

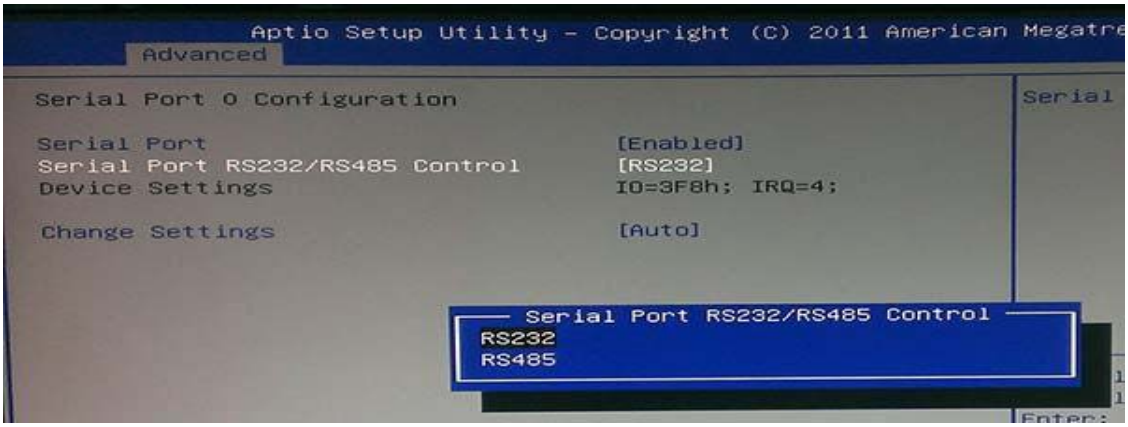
| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | WDT_PME | R | -- | The PME Status |
| | | | | This bit will set when WDT_PME_EN is set and the |
| | | | | watchdog timer is 1 unit before time out (of time out) |
| 6 | WDT_PME_EN | R/W | 0 | 0 : Disable Watchdog PME. |
| | | | | 1 : Enable Watchdog PME |
| 5-1 | Reserved | -- | -- | Reserved |
| 0 | WDOUT_EN | R/W | 0 | 0 : disable Watchdog time out output via WDTRST# |
| | | | | 1 : enable Watchdog time out output via WDTRST# |

# 6.0 BIOS Setting

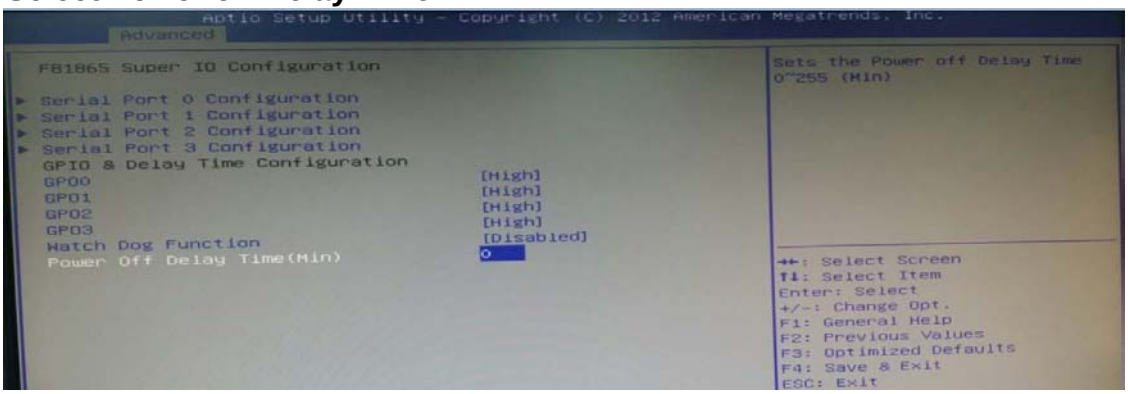
## Super IO Configuration




## Select Serial Port Mode




## Select Power off Delay Time

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# Technical Support:

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